



User's Guide

NHD-0440AZ-NLY-FBW-C6

LCM

(Liquid Crystal Display Character Module)

FEATURES

- Display format: 4 Lines x 40 Characters
- **(A)** – Display Series/Model
- **(Z)** – Factory line
- **(N)** - Polarizer = Transmissive (-) light method
- **(LY)** – Backlight = LED (Yellow-Green)
- **(F)** – LCD Type = FSTN
- **(B)** – View Direction = 6:00
- **(S/W)** – Operating Temp. = Standard (0 ~ +50c) , Wide (-20 ~ +70c)

LCD driver IC: SPLC780D

(C) - 2x8 Pin FCI part#: 88874-016, shrouded header, 30u gold, right-angle, lead free, 5.84mm mating length.

Header soldered onto component side of LCD PCB.

(6) - R6 = 3.3K ohm Resistor

For product support, contact

Newhaven Display International, LLC
2511 Technology Drive, #101
Elgin, IL 60124

Tel: (847) 844-8795 Fax: (847) 844-8796

February 01, 2008

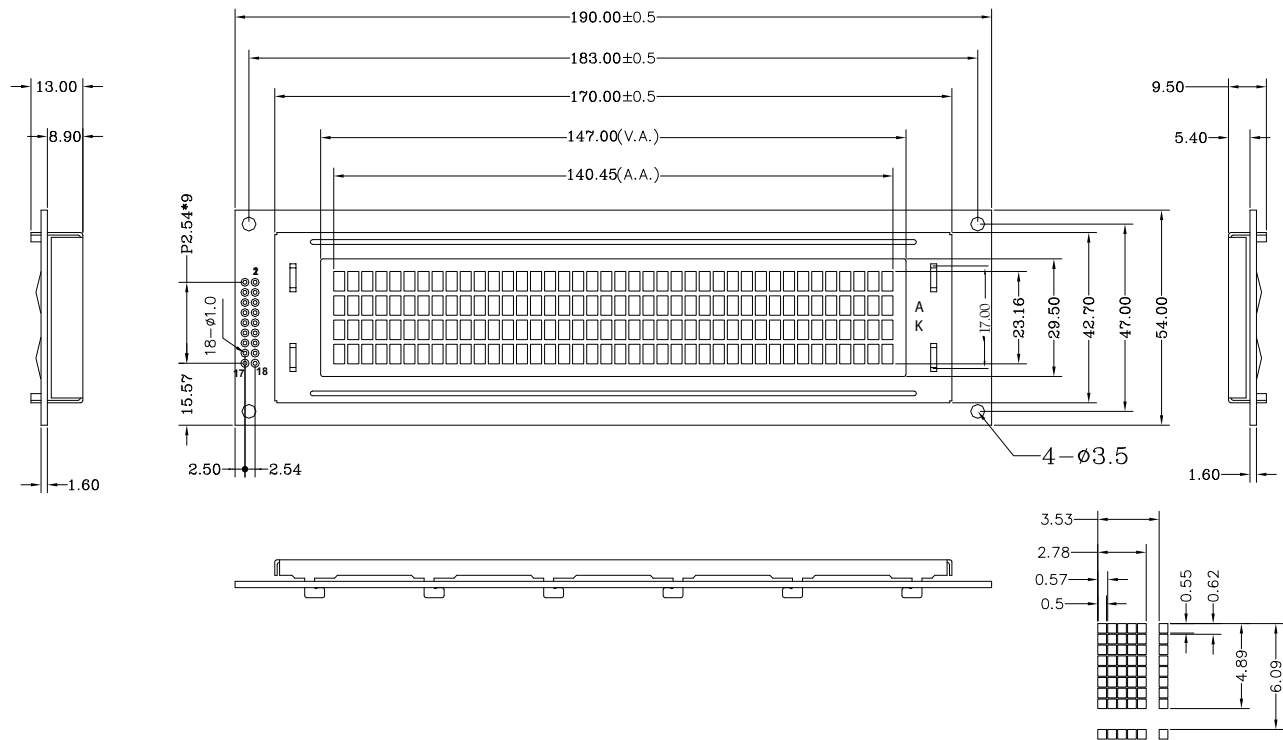
NHD0440AZ-NLY-FBW-C6

SPECIFICATIONS OF LCD MODULE

Features

1. 5x8 dots with cursor
2. Display format: 40characters * 4 lines
3. Built-in controller (SPLC780D)
4. +5V power supply
5. 1/16 duty, 1/5 bias cycle
6. FSTN, Transmissive negative display
7. Viewing direction: 6:00 o'clock

Outline dimension



Absolute maximum ratings

Item	Symbol	Standard			Unit
Power voltage	$V_{DD}-V_{SS}$	0	-	7.0	V
Input voltage	V_{IN}	V_{SS}	-	V_{DD}	
Operating temperature range	V_{OP}	-20	-	+70	C
Storage temperature range	V_{ST}	-30	-	+80	

*Wide temperature range is available

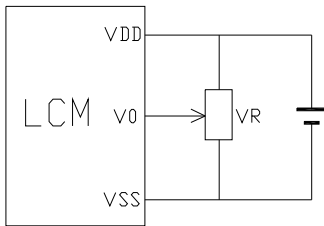
NHD-0440AZ

Interface pin description

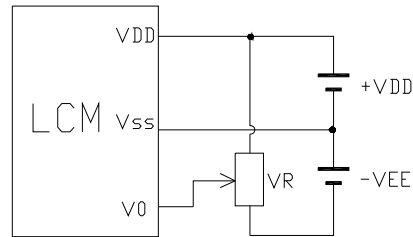
Pin no.	Symbol	External connection	Function
1~4	DB7~DB4	MPU	Four high order bi-directional three-state data bus lines. Used for data transfer between the MPU
5~8	DB3~DB0	MPU	Four low order bi-directional three-state data bus lines. Used for data transfer between the MPU and the LCM. These four are not used during 4-bit operation.
9	E1	MPU	Operation (data read/write) enable signal
10	R/W	MPU	Read/write select signal
11	RS	MPU	Register select signal
12	V ₀	Power supply	Contrast adjust
13	V _{SS}		Signal ground for LCM (GND)
14	V _{DD}		Power supply for logic (+5V) for LCM
15	E2	MPU	Enable signal (no pull-up resistor)
16	NC		
A	A	Power supply	Power supply for LED backlight (+4.2V)
K	K		Power supply for LED backlight (0V)

Contrast adjust

A) For Single Source



B) For Double Source

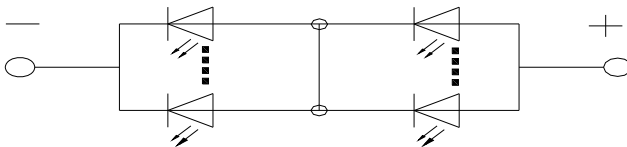


V_{DD}-V₀: LCD Driving voltage

VR: 1k~2k

Electrical characteristics

Backlight circuit diagram (light 48 x 2)



led ratings (Yellow/Green)

(UAK = 4.2V, Ta =25°C)

Item	Symbol	Min	Typ.	Max	Unit
Forward Voltage	VAK	3.6	4.2	4.3	V
Forward current	I _f	-	480	500	mA
Power	P			2016	mW
Peak wave length	λ _p		570		nm
Luminance	L _v		80		Cd/m ²

NHD-0440AZ

FSTN type display module (Ta=25°C, VDD=5.0V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Viewing angle	θ	$C_r \geq 2$	-60	-	35	deg
	Φ		-40	-	40	
Contrast ratio	C_r		-	6	-	-
Response time (rise)	T_r	-	-	150	250	ms
Response time (fall)	T_r	-	-	150	250	

Electrical characteristics

DC characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage for LCD	$V_{DD}-V_0$	Ta=25°C	-	5.0	-	V
Input voltage	V_{DD}		2.7	-	5.5	
Supply current	I_{DD}	Ta=25°C, VDD=5.0V	-	3.5	4.0	mA
Input leakage current	I_{LKG}		-	-	5.0	uA
“H” level input voltage	V_{IH}		2.2	-	V_{DD}	V
“L” level input voltage	V_{IL}	Twice initial value or less	0	-	0.6	
“H” level output voltage	V_{OH}	LOH=-0.25mA	2.4	-	-	
“L” level output voltage	V_{OL}	LOH=1.6mA	-	-	0.4	
Backlight supply voltage	V_F		-	-	5.0	
Backlight supply current	I_F	$V_F=4.2V$	-	480	-	mA

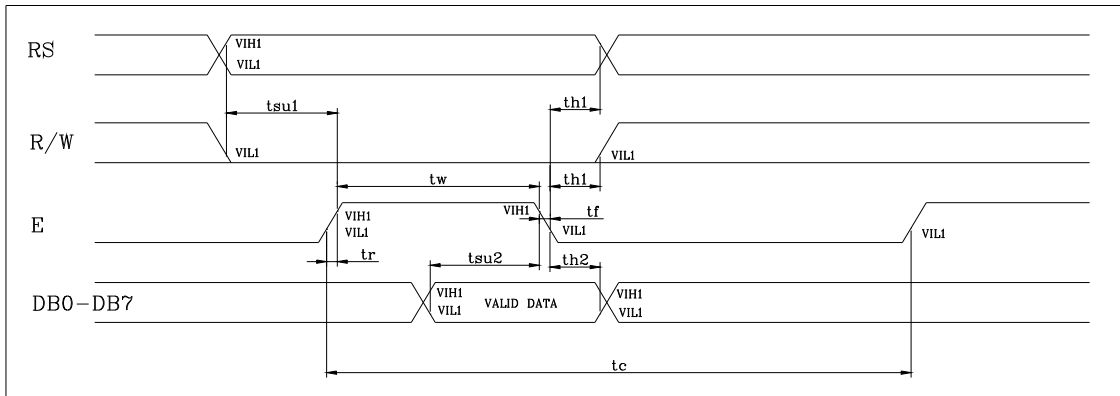
Read cycle (Ta=25°C, VDD=5.0V)

Parameter	Symbol	Test pin	Min.	Typ.	Max.	Unit
Enable cycle time	t_c	E	500	-	-	ns
Enable pulse width	t_w		300	-	-	
Enable rise/fall time	t_r, t_f		-	-	25	
RS; R/W setup time	t_{su}	RS; R/W	100	-	-	
RS; R/W address hold time	t_h	RS; R/W	10	-	-	
Read data output delay	t_d	DB0~DB7	60	-	90	
Read data hold time	t_{dh}		20	-	-	

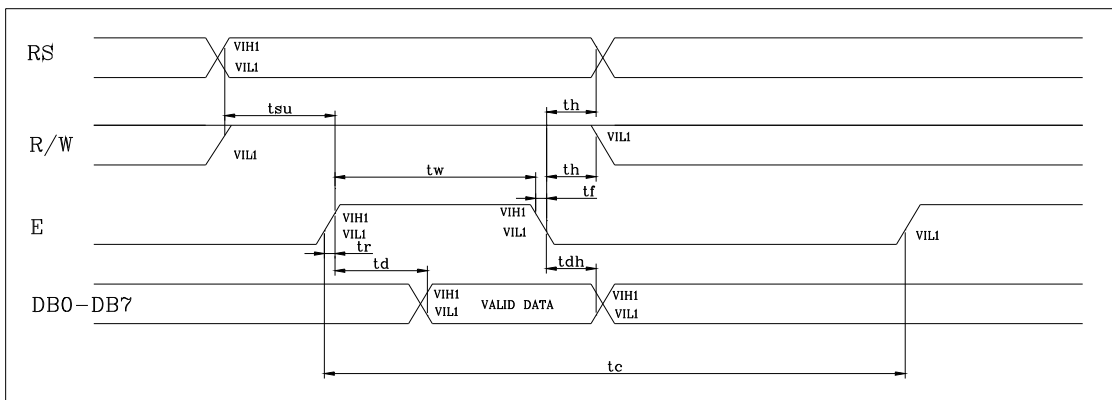
Write cycle (Ta=25°C, VDD=5.0V)

Parameter	Symbol	Test pin	Min.	Typ.	Max.	Unit
Enable cycle time	t_c	E	500	-	-	ns
Enable pulse width	t_w		300	-	-	
Enable rise/fall time	t_r, t_f		-	-	25	
RS; R/W setup time	t_{su1}	RS; R/W	100	-	-	
RS; R/W address hold time	t_{h1}	RS; R/W	10	-	-	
Read data output delay	t_{su2}	DB0~DB7	60	-	-	
Read data hold time	t_{h2}		10	-	-	

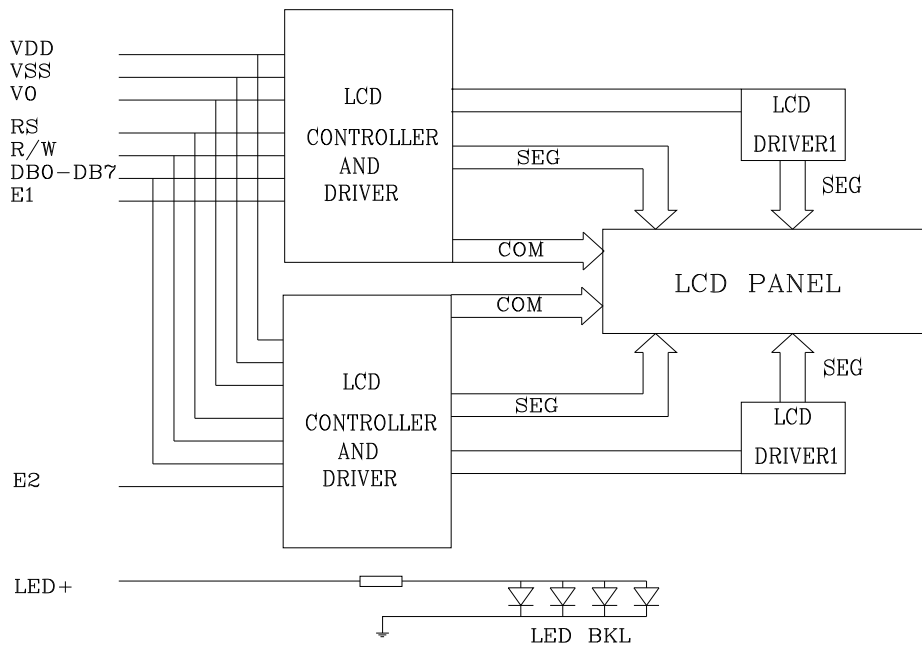
Write mode timing diagram



Read mode timing diagram



Block diagram



Instruction description

Outline

To overcome the speed difference between the internal clock of KS0066U and the MPU clock, KS0066U performs internal operations by storing control in formations to IR or DR. The internal operation is determined according to the signal from MPU, composed of read/write and data bus (Refer to Table7).

Instructions can be divided largely into four groups:

- 1) KS0066U function set instructions (set display methods, set data length, etc.)
- 2) Address set instructions to internal RAM
- 3) Data transfer instructions with internal RAM
- 4) Others

The address of the internal RAM is automatically increased or decreased by 1.

Note: during internal operation, busy flag (DB7) is read “High”.

Busy flag check must be preceded by the next instruction.

When an MPU program with checking the busy flag (DB7) is made, it must be necessary 1/2 fuss for executing the next instruction by the falling edge of the “E” signal after the busy flag (DB7) goes to “LOW”.

Contents

- 1) Clear display

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1

Clear all the display data by writing “20H” (space code) to all DDRAM address, and set DDRAM address to “00H” into AC (address counter).

Return cursor to the original status, namely, brings the cursor to the left edge on the fist line of the display.

Make the entry mode increment (I/D=“High”).

- 2) Return home

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	-

Return home is cursor return home instruction.

Set DDRAM address to “00H” into the address counter.

Return cursor to its original site and return display to its original status, if shifted.

Contents of DDRAM does not change.

- 3) Entry mode set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	I/D	SH

Set the moving direction of cursor and display.

I/D: increment / decrement of DDRAM address (cursor or blink)

When I/D=“high”, cursor/blink moves to right and DDRAM address is increased by 1.

When I/D=“Low”, cursor/blink moves to left and DDRAM address is increased by 1.

*CGRAM operates the same way as DDRAM, when reading from or writing to CGRAM.

(I/D=“high”. shift left, I/D=“Low”. Shift right).

4) Display ON/OFF control

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	D	C	B

Control display/cursor/blink ON/OFF 1 bit register.

D: Display ON/OFF control bit

When D="High", entire display is turned on.

When D="Low", display is turned off, but display data remains in DDRAM.

C: cursor ON/OFF control bit

When D="High", cursor is turned on.

When D="Low", cursor is disappeared in current display, but I/D register preserves its data.

B: Cursor blink ON/OFF control bit

When B="High", cursor blink is on, which performs alternately between all the "High" data and display characters at the cursor position.

When B="Low", blink is off.

5) Cursor or display shift

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	S/C	R/L	-	-

Shifting of right/left cursor position or display without writing or reading of display data.

This instruction is used to correct or search display data. (Refer to Table 6)

During 2-line mode display, cursor moves to the 2nd line after the 40th digit of the 1st line.

When display data is shifted repeatedly, each line is shifted individually.

When display shift is performed, the contents of the address counter are not changed.

Shift patterns according to S/C and R/L bits

S/C	R/L	Operation
0	0	Shift cursor to the left, AC is decreased by 1
0	1	Shift cursor to the right, AC is increased by 1
1	0	Shift all the display to the left, cursor moves according to the display
1	1	Shift all the display to the right, cursor moves according to the display

6) Function set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	DL	N	F	-	-

DL: Interface data length control bit

When DL="High", it mans 8-bit bus mode with MPU.

When DL="Low", it mans 4-bit bus mode with MPU. Hence, DL is a signal to select 8-bit or 4-bit bus mode.

When 4-bit bus mode, it needs to transfer 4-bit data twice.

N: Display line number control bit

When N="Low", 1-line display mode is set.

When N="High", 2-line display mode is set.

NHD-0440AZ

F: Display line number control bit

When F="Low", 5x8 dots format display mode is set.

When F="High", 5x11 dots format display mode.

7) Set CGRAM address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

Set CGRAM address to AC.

The instruction makes CGRAM data available from MPU.

8) Set DDRAM address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0

Set DDRAM address to AC.

This instruction makes DDRAM data available from MPU.

When 1-line display mode (N=LOW), DDRAM address is form "00H" to "4FH".

In 2-line display mode (N=High), DDRAM address in the 1st line form "00H" to "27H", and DDRAM address

In the 2nd line is from "40H" to "67H".

9) Read busy flag & address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0

This instruction shows whether KS0066U is in internal operation or not.

If the resultant BF is "High", internal operation is in progress and should wait BF is to be LOW, which by then if the next instruction can be performed. In this instruction you can also read the value of the address counter.

10) Write data to RAM

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	D7	D6	D5	D4	D3	D2	D1	D0

Write binary 8-bit data to DDRAM/CGRAM.

The selection of RAM from DDRAM, and CGRAM, is set by the previous address set instruction (DDRAM address set, CGRAM address set).

RAM set instruction can also determine the AC direction to RAM.

After write operation. The address is automatically increased/decreased by 1, according to the entry mode.

11) Read data from RAM

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	D7	D6	D5	D4	D3	D2	D1	D0

Read binary 8-bit data from DDRAM/CGRAM.

The selection of RAM is set by the previous address set instruction. If the address set instruction of RAM is not performed before this instruction, the data that has been read first is invalid, as the direction of AC is not yet determined. If RAM data is read several times without RAM address instructions set before, read operation, the correct RAM data can be obtained from the second. But the first data would be incorrect, as there is no time margin to transfer RAM data.

In case of DDRAM read operation, cursor shift instruction plays the same role as DDRAM address set instruction,

It also transfers RAM data to output data register.

After read operation, address counter is automatically increased/decreased by 1 according to the entry mode.

After CGRAM read operation, display shift may not be executed correctly.

NOTE: In case of RAM write operation, AC is increased/decreased by 1 as in read operation.

At this time, AC indicates next address position, but only the previous data can be read by the read instruction.

Instruction table

Instruction	Instruction code										Description	Execution Time (fosc= 270 KHZ)	
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0			
Clear Display	0	0	0	0	0	0	0	0	0	0	1	Write "20H" to DDRA and set DDRAM address to "00H" from AC	1.53ms
Return Home	0	0	0	0	0	0	0	0	0	1	-	Set DDRAM address to "00H" From AC and return cursor to Its original position if shifted. The contents of DDRAM are not changed.	1.53ms
Entry mode Set	0	0	0	0	0	0	0	0	1	I/D	SH	Assign cursor moving direction And blinking of entire display	39us
Display ON/OFF control	0	0	0	0	0	0	0	1	D	C	B	Set display (D), cursor (C), and Blinking of cursor (B) on/off Control bit.	
Cursor or Display shift	0	0	0	0	0	0	1	S/C	R/L	-	-	Set cursor moving and display Shift control bit, and the Direction, without changing of DDRAM data.	39us
Function set	0	0	0	0	1	DL	N	F	-	-	-	Set interface data length (DL: 8-Bit/4-bit), numbers of display Line (N: =2-line/1-line) and, Display font type (F: 5x11/5x8)	39us
Set CGRAM Address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0		Set CGRAM address in address Counter.	39us
Set DDRAM Address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0		Set DDRAM address in address Counter.	39us
Read busy Flag and Address	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0		Whether during internal Operation or not can be known By reading BF. The contents of Address counter can also be read.	0us
Write data to Address	1	0	D7	D6	D5	D4	D3	D2	D1	D0		Write data into internal RAM (DDRAM/CGRAM).	43us
Read data From RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0		Read data from internal RAM (DDRAM/CGRAM).	43us

NOTE: When an MPU program with checking the busy flag (DB7) is made, it must be necessary 1/2fosc is necessary for executing the next instruction by the falling edge of the "E" signal after the busy flag (DB7) goes to "Low".

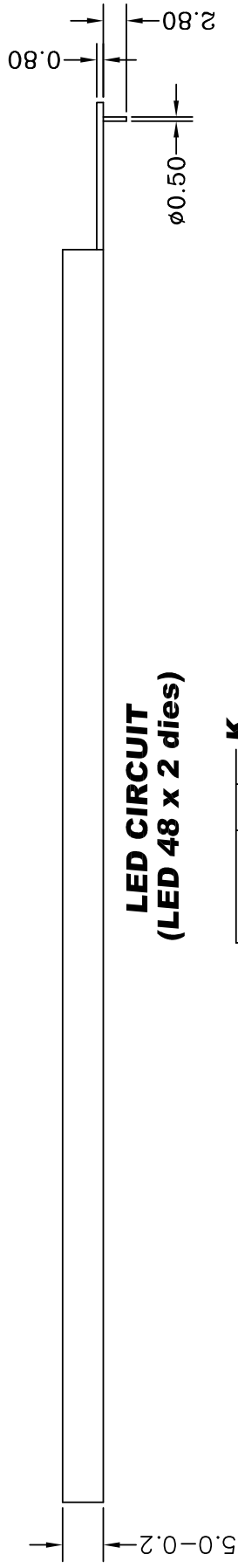
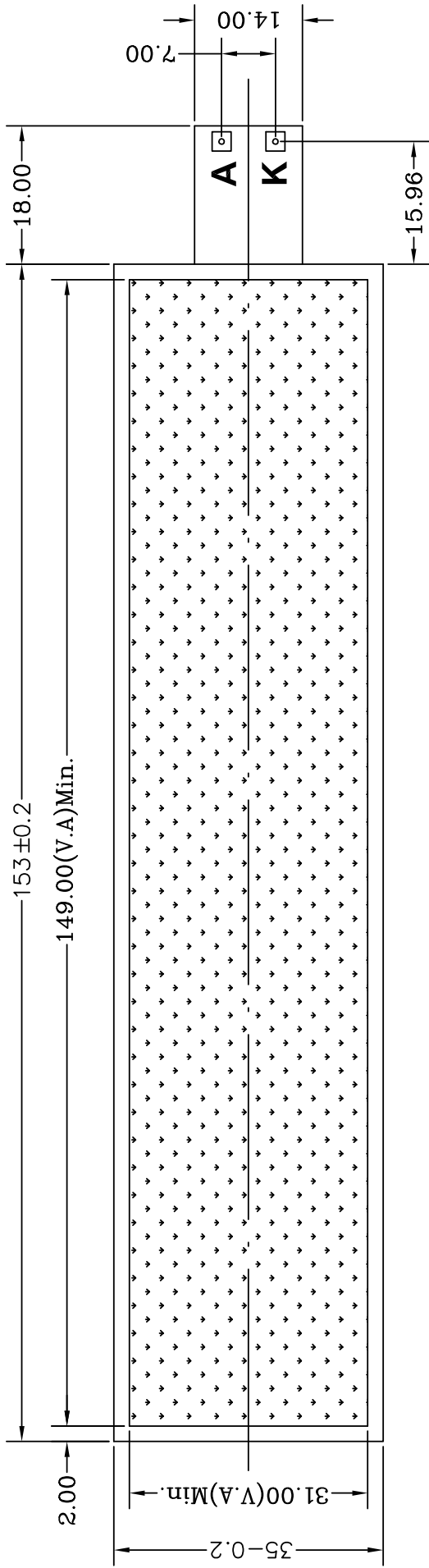
DDRAM address:

															Display position				
1	2	3	4	5	-	-	-	-	-	-	-	-	-	-	36	37	38	39	40
00	01	02	03	04	-	-	-	-	-	-	-	-	-	-	23	24	25	26	27
40	40	41	42	43	-	-	-	-	-	-	-	-	-	-	63	64	65	66	67
00	01	02	03	04	-	-	-	-	-	-	-	-	-	-	23	24	25	26	27
40	40	41	42	43	-	-	-	-	-	-	-	-	-	-	63	64	65	66	67

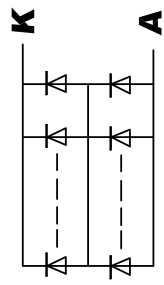
DDRAM address

Standard character pattern

Lower 4 Bits \ Upper 4 Bits	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
xxxx0000	CG RAM (1)		0	1	2	3	4	5	6			7	8	9	0	1
xxxx0001	(2)		!	1	A	Q	a	q			.	7	8	9	0	1
xxxx0010	(3)		"	2	B	R	b	r			[イ	ツ	×	β	θ
xxxx0011	(4)		#	3	C	S	c	s]	ウ	テ	モ	ε	∞
xxxx0100	(5)		\$	4	D	T	d	t			\	エ	ト	ホ	μ	Ω
xxxx0101	(6)		%	5	E	U	e	u			.	オ	ナ	1	ε	Ω
xxxx0110	(7)		&	6	F	V	f	v			ヲ	カ	ニ	ヨ	ρ	Σ
xxxx0111	(8)		'	7	G	W	g	w			ア	キ	ヌ	ラ	g	π
xxxx1000	(1)		(8	H	X	h	x			イ	ク	ネ	リ	フ	Σ
xxxx1001	(2))	9	I	Y	i	y			ウ	ケ	ル	ル	'	g
xxxx1010	(3)		*	:	J	Z	j	z			エ	コ	ン	レ	j	キ
xxxx1011	(4)		+	;	K	[k	(オ	サ	ヒ	ロ	°	ホ
xxxx1100	(5)		,	<	L	¥	l				ホ	シ	フ	フ	¢	円
xxxx1101	(6)		-	=	M]	m)			ユ	ヌ	ヘ	ン	モ	÷
xxxx1110	(7)		.	>	N	^	n	÷			ヨ	セ	ホ	°	ん	
xxxx1111	(8)		/	?	O	_	o	+			ッ	リ	マ	°	ö	■



**LED CIRCUIT
(LED 48 x 2 dies)**



- NOTES:**
- 1.LED TYPE:(96 LEDS, MATRIX)
 - 2.CIUCUIT TYPE: SERIES-PARALLEL
 - 3.COLOUR: YELLOW-GREEN
 - 4.PEAK WAVE LENGTH: 565nm-570nm
 - 5.SUPPLY VOLTAGE: 3.8 V - 4.4V
 - 6.CURRENT: 480mA-720mA
 - 7.LUMINOUS INTENSITY: 110 cd/m² 85cd/m² (MIN)
 - 8.OPERATION TEMP: -20°C TO 70°C
 - 9.STORAGE TEMP: -25°C TO 75°C
 - 10.UNIFORMLY: 75%(MIN)
 - 11.UNMARKED TOLERANCES:± 0.2mm

E.L.A(Effective Light Area)

UNIT: mm

Newhaven Display International, LLC					
REVISION RECORD			Drawn:	Model Name:	
VER	Date	Modify	Contents	Name	Confirm
2					
3					
4					
5					
6					

Date: 2004-01-07
Checker:
Approved:
Page: 1-1

ENGINEERING CHANGE NOTICE

[] PART NUMBER ACTION NOTICE

of C'd's/Disks attached: _____
Drawing #: _____

ECN NO 09333

VENDOR NAME _____

ORIG HARRY

VENDOR PART # _____

ENG / REQ FREDDY

MANUFACTURER FCI ELECTRONICS

NPI PART 01909181

MFG PART # 88874-016

DESC CONNECTOR-HEADER-16 PIN-RA-WV

APPROX COST _____

END WINDOWS _____

PROJECT Commercial

CREATE/UPDATE BOM (Only for BOM) YES NO
 NEW RELEASE YES NO
 UPDATE YES NO

CURRENT REVISION A NEW REVISION 29P

DPT. RESPONSIBLE FOR DRAWING ME EE SE

DESCRIPTION OF CHANGE & WHY
(IF NEEDED FOR CLARITY, ATTACH A MARKED-UP COPY OF DRAWING)

CAF# _____ DRAFTER: _____ DATE: _____

UPDATE SPEC

PLEASE ADD MANUFACTURE 3M AND P.N. 2516-5002UB AS ALTERNATE TO THIS NUMBER

VENDOR HAS BEEN NOTIFIED FIX REPORTED PROBLEM CE EFFECTIVITY: NO EFFECT SAFETY EMC

FOR DDC USE ONLY

CN HAND	OPEN I/O & B/O			FINISHED GOODS			OPEN I/O - WIP			FIELD			SPARES		
	UPDATE	CANCEL	NO EFFECT	UPDATE	CANCEL	NO EFFECT	REWORK	SCRAP	NO EFFECT	REWORK	SCRAP	NO EFFECT	REWORK	SCRAP	NO EFFECT
REWORK															
SCRAP															
NO EFFECT	<input checked="" type="checkbox"/>														

RECEIVED

JAN 03 2005

ENTERED
B 14 05

DEPARTMENT	APP DATE	SIGNATURE	REV DATE	SIGNATURE	COMMENTS
ENGINEER	1/3/05	<i>[Signature]</i>			
ENGINEERING DPT MANAGER	1-3-05	<i>[Signature]</i>			
VP OF ENGINEERING					
PROJECT MANAGER					
DOCUMENT CTRL MANAGER	1-4-05	<i>[Signature]</i>			
CUSTOMER SERVICE MANAGER					

REVISED
1/14/05

2 of 4

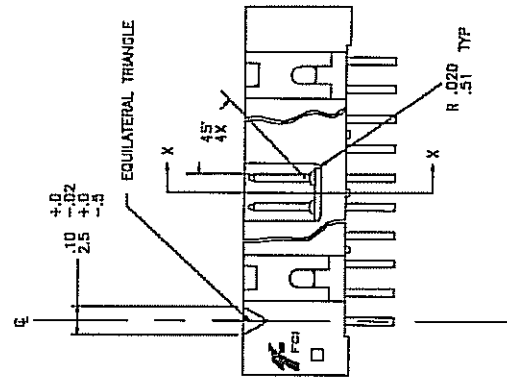
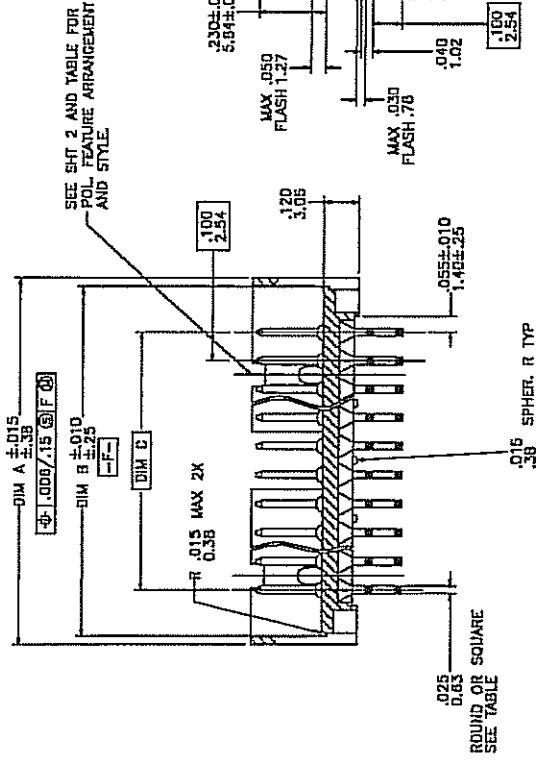
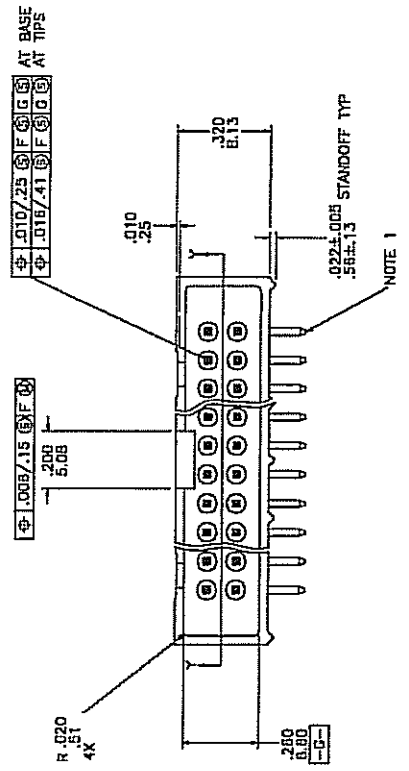
1

2

3

4

PRODUCT NUMBER
SEE TABLE



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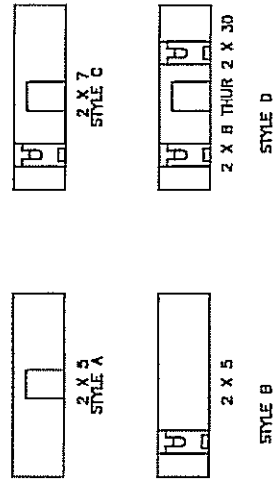
SEE NOTE 2		Tolerances unless otherwise specified		CUSTOMER COPY		Electronics	
U	FCI	FCI	www.fcimanufact.com	FCI		www.fcimanufact.com	
A	V1921	JM	B/13/91	linear	.XXX ±.005/0.13	HEADER QUICKIE SLIM LINE	
B	V12776	JM	10/14/91	projection	XXXX ±.0020/0.05	RIGHT ANGLE 4-WALLED	
C	V40786	MSC	5/31/94	projection	0 ±.2	product family	
D	V20288	RGD	2/7/02	dr	JMAUSTARD B/13/91	size dwg no	
				enrg	WFLUNK B/13/91	code	
				chr	M.SMYK B/13/91	sheet	
				appd	M.SMYK B/13/91	1 of 3	
sheet	revision	D	D	D		A	
Index	sheet	1	2	3		88874	
						code	
						22526	
						4	

ACAD

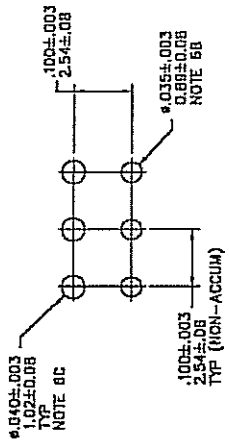
3 of 4

1 | 2 | 3 | 4

PRODUCT NUMBER
SEE TABLE



X	TERMINAL PLATING	DIM S ±.01	TERMINAL TYPE
-0XX	30u"/76u Au OVER 50u"/1.27u Ni	.105/2.67	RD
-1XX	30u"/76u CrT/GOLD FLASH	.105/2.67	RD
-2XX	30u"/76u Au OVER 50u"/1.27u Ni	.150/3.81	RD
-3XX	30u"/76u CrT/GOLD FLASH	.150/3.81	RD
-4XX	30u"/76u Au OVER 50u"/1.27u Ni	.105/2.67	SQ
-5XX	15u"/38u CrT/GOLD FLASH	.105/2.67	SQ
-6XX	30u"/76u Au OVER 50u"/1.27u Ni	.150/3.81	SQ
-7XX	30u"/76u CrT/GOLD FLASH	.150/3.81	SQ
-8XX	15u"/38u Au OVER 50u"/1.27u Ni	.150/3.81	SQ
-9XX	30u"/76u CrT/GOLD FLASH	.105/2.67	SQ



RECOMMENDED HOLE PATTERN
SCALE 10/1

NOTES:

- SAME PIN POSITION TOLERANCE APPLIES TO BOTH ENDS OF EACH TERMINAL.
- MOLDING MAT'L: 30% GLASS-FILLED POLYESTER, FLAME RETARDANT PER UL-94V-0, COLOR: BLUE.
1. MAX DRAFT PERMISSIBLE ON ALL SURFACES.
- 4 POUNDS/1.8 KILOGRAMS MIN. TERM. PULL-OUT FORCE.
- TERMINAL MAT'L: PHOSPHOR BRONZE.
- A. PART NUMBERS HAVING AN "R" FOLLOWING THE B DIGIT PART NUMBER (EXAMPLE BR23R-010R) HAVE TWO PAIRS OF PINS AT EACH END TO PROVIDE RETENTION. LOCATION IS MANUFACTURER'S OPTION. SEE DETAIL "H" SHEET 1.
- CONNECTORS WITH RETENTION AND ROUND PINS HAVE 15LB./6.8KG. MAX INSERTION AND 25LB./11KG. MIN. RETENTION FORCE WHEN USED IN A .035/0.98±.003/0.08 DIA HOLE AND .062/1.58 THICK P.C.BOARD.
- CONNECTORS WITH RETENTION AND SQUARE PINS HAVE A 15LB./6.8KG. MAX INSERTION AND A .5LB./23KG. MIN RETENTION WHEN USED IN A .040/1.02±.003/0.08 DIA HOLE AND A .062/1.58 THICK P.C.BOARD.

mult. code	tolerances unless otherwise specified	CUSTOMER COPY	Electronics F.C.I.
SEE NOTE 2	linear .XX ±.01/.3	projection	www.electronics.com
lit. sec. no.	.XXX ±.005/0.13	INCH/MM	HEADER QUICKIE SLIM LINE
dir.	XXXX ±.0020/0.05	0 ±.2°	RIGHT ANGLE 4-WALLED
dr.	J.MUSTARD 18/13/91	product family	OKE
crq.	W.FUNK 6/13/91	size dwg no.	code
chr.	M.SARK 18/13/91	scale	88874
app.	M.SARK 18/13/91	5:1	sheet 2 of 4
revision sheet			code code 22526
Index			

ACAD

4 084

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PRODUCT NUMBER	POS	DIM A	DIM B	DIM C	STYLE
NOTE 6					
88874-X02	2X5	.78/18.8	.72/18.3	.400/10.16	B
-X08	2X4	.68/17.3	.62/15.8	.300/7.62	A
-X10	2X5	.78/19.8	.72/18.3	.400/10.16	A
-X14	2X7	.98/24.9	.92/23.4	.600/15.24	C
-X16	2X8	1.08/27.8	1.02/25.9	.700/17.78	D
-X20	2X10	1.28/32.5	1.22/31.0	.800/22.86	
-X24	2X12	1.48/37.6	1.42/36.1	1.100/27.94	
-X28	2X13	1.58/40.1	1.52/38.6	1.200/30.48	
-X30	2X15	1.78/45.2	1.72/43.7	1.400/35.56	
-X34	2X17	1.98/50.3	1.92/48.8	1.600/40.84	
-X40	2X20	2.28/57.9	2.22/56.4	1.900/48.26	
-X44	2X22	2.48/63.0	2.42/61.5	2.100/53.34	
-X50	2X25	2.78/70.6	2.72/68.1	2.400/60.96	
88874-X60	2X30	3.28/83.3	3.22/81.8	2.900/73.66	D

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FCI

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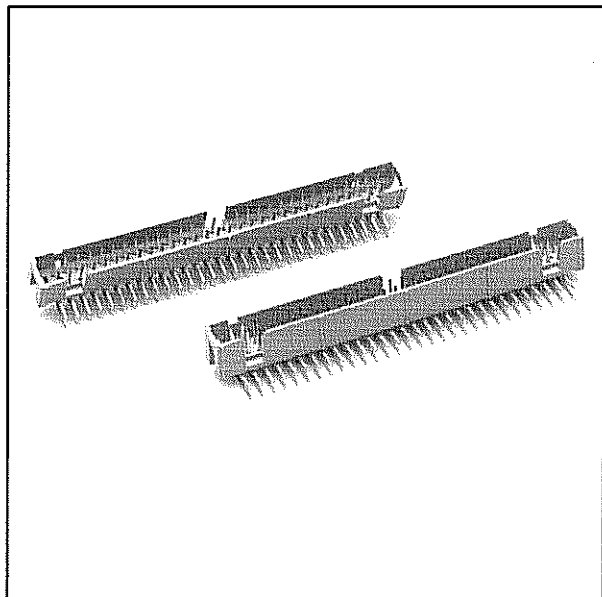
mat'l. code SEE NOTE 2		tolerances unless otherwise specified		CUSTOMER COPY		Electronics FCI www.fciconnect.com	
ltr	acn no	linear	.XX ±.01/3	projection	product family	code	
D		angular	.XXX ±.005/0.13		HEADER QUICKIE SLIM LINE	sheet	
		dr	.XXXX ±.0020/0.05		RIGHT ANGLE 4-WALLED	3 of	
		enrgt	σ ±.7	INCH/MM	product family	size	
		chr	J.MUSTARD 8/13/91	5:1	OKE	A	
		suppl	W.FUNK 8/13/91		product family	88874	
		revision	M.SARK 8/13/91		size		
sheet		sheet	M.SARK 8/13/91		code		
index							

1 | 2 | 3 | 4

ACAD

3M™ Pak 100 4-Wall Header

.100" × .100" Low Profile, Straight and Right Angle, High Temp Option 2500 Series



- Low profile, space saving design
- Socket compatibility for current design validation
- Center slot polarization prevents mis-insertions and reduces insertion time
- Dual slot polarization means broader compatibility with competitive polarization designs
- Optional retainer clamp for locking sockets in place and increasing connection reliability in vibration-prone environments
- Optional snap-in latches available
- Optional polarizing post available
- Exposed solder tails (on right angle version) provide ease of cleaning and reduced repair costs

Date Modified: May 30, 2003

TS-0770-11
Sheet 1 of 3

Physical

Insulation

Material: Glass Filled Polyester (PBT)
Glass Filled Polyester (PCT) (High Temp Option)

Flammability: UL 94V-0

Color: Gray
Beige (High Temp Option)

Contact

Material: Copper Alloy

Plating

Underplate: 100 μ " [2.54 μ m] Nickel — QQ-N-290, Class 2
Wiping Area: Gold — MIL-G-45204, Type II, Grade C
Solder Tails: 200 μ " [5.08 μ m] 60/40 Tin Lead — MIL-P-81728
Wrap Tails: Gold Flash (Normal Temp Only)

Marking: 3M Logo, and Orientation Triangle

Electrical

Current Rating: 2 A

Insulation Resistance: $>1 \times 10^9 \Omega$ at 500 Vdc

Withstanding Voltage: 1000 Vrms at Sea Level

Environmental

Temperature Rating: -55°C to +105°C

Processing: Maximum 235°C, with 90 seconds over 215°C (High Temp Option)

UL File No.: E68080

3M

Interconnect Solutions

<http://www.3M.com/interconnects/>

3M is a trademark of 3M Company.

For technical, sales or ordering information call

800-225-5373

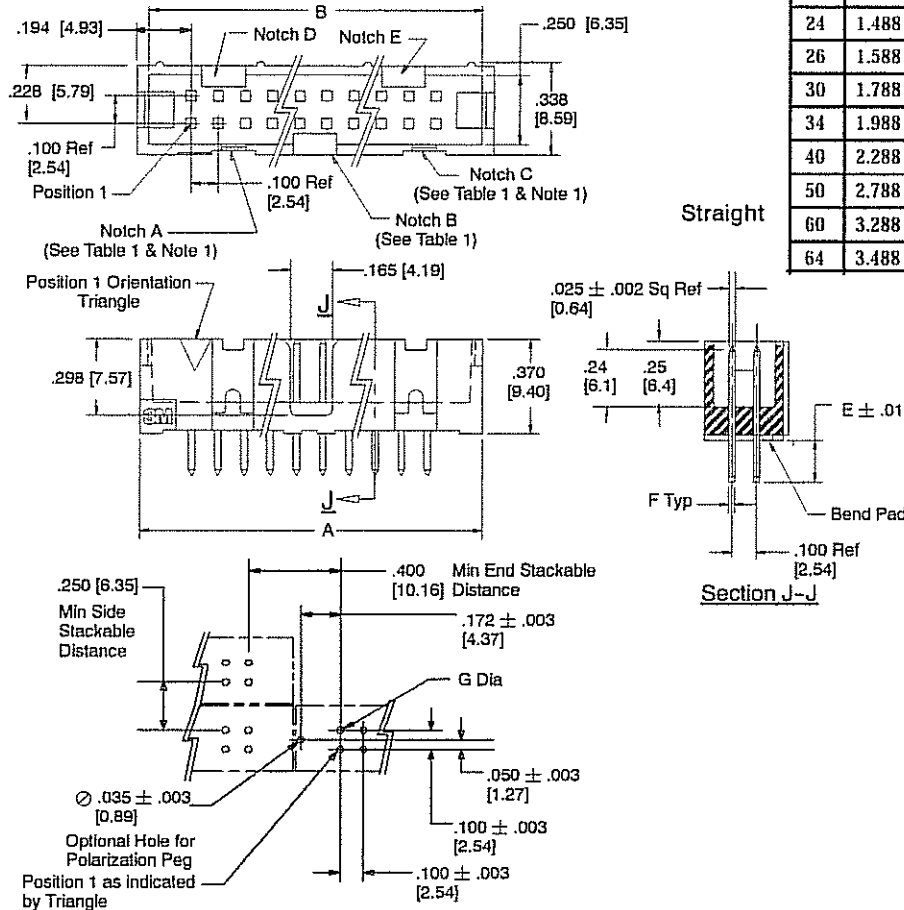
3M™ Pak 100 4-Wall Header

.100" × .100" Low Profile, Straight and Right Angle, High Temp Option

2500 Series

Tail	Dim E	Pin Cross Section			Dim G ± .003
		Dimension F	Diagonals	Corner Radii	
X2	.112 [2.84]	.0245 ± .0005 [0.622]	.028 ± .001 [0.71]	.0075 Ref [0.191]	.035 [0.89] (See Note 2)
03	.155 [3.94]	.0245 ± .0005 [0.622]	.028 ± .001 [0.71]	.0075 Ref [0.191]	.035 [0.89]
05	.61 Ref [15.5]	.0250 ± .002 [0.635]	.035 ± .003 [0.90]	.003 Max [0.08]	.045 [1.14]

Pin Qty	Dimensions		Polarizing Notches
	A	B	
10	.788 [20.02]	.708 [17.98]	BC
14	.988 [25.10]	.908 [22.06]	BCDE
16	1.088 [27.64]	1.008 [25.60]	ABCDE
20	1.288 [32.72]	1.208 [30.68]	ABCDE
24	1.488 [37.80]	1.408 [35.76]	ABCDE
26	1.588 [40.34]	1.508 [38.30]	ABCDE
30	1.788 [45.42]	1.708 [43.38]	ABCDE
34	1.988 [50.50]	1.908 [48.46]	ABCDE
40	2.288 [58.12]	2.208 [56.08]	ABCDE
50	2.788 [70.82]	2.708 [68.78]	ABCDE
60	3.288 [83.52]	3.208 [81.48]	ABCDE
64	3.488 [88.60]	3.408 [86.56]	ABCDE



Tolerance Unless Noted			
	.0	.00	.000
Inch	± .1	± .01	± .005

- Notes:
- Notches "A" and "C" will accommodate 3M Polarizing Keys 3518.
 - The recommended PCB hole size for the kinked tail positions on the .112" solder tail connector is .035" ± .002. Refer to TS-0972 for the positions kinked.

Ordering Information

X25XX-X0XXXX

Blank = Standard	<p>Mating Plating Thickness: Solder Tail Versions UG = 15 μ" [0.38 μm] UB = 30 μ" [0.76 μm] Wrap Tail Versions EB = 30 μ" [0.76 μm] (Normal temp Only)</p> <p>TS-0770-11 Sheet 2 of 3</p>
N = High Temperature	
Pin Quantity: (See Table 1)	
Bend Pad Option: 6= Straight pin product with bend pad in High temp or normal plastics 7= Straight pin product w/o bend pad in High temp only	
Tail	<p>02 = Solder Tails for .062 [1.57] Thick Board. K2 = Kinked Solder Tails for .062 [1.57] Thick Board. 03 = Solder Tails for .094 to .125 [2.39 to 3.18] Thick Board. 05 = Wrap Tails for up to 3 Levels of Wire Wrap. (Normal temp only)</p>

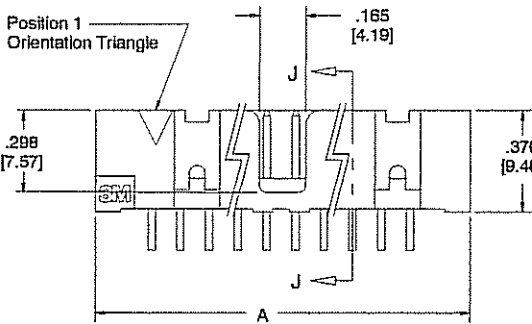
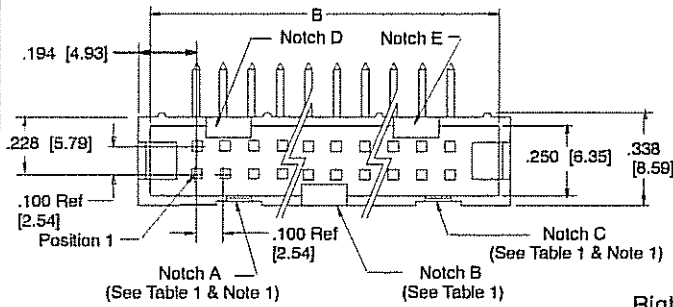
3M™ Pak 100 4-Wall Header

.100" × .100" Low Profile, Straight and Right Angle, High Temp Option

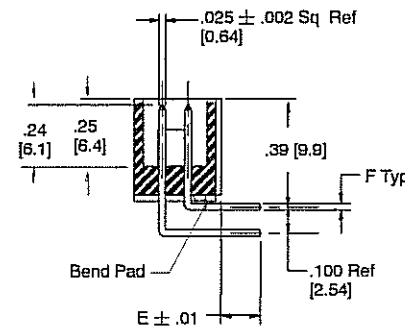
2500 Series

Tail	Dim E	Pin Cross Section			Dim G ± .003
		Dimension F	Diagonals	Corner Radii	
X2	.112 [2.84]	.0245 ± .0005 [0.622]	.028 ± .001 [0.71]	.0075 Ref [0.191]	.035 [0.89] (See Note 2)
03	.155 [3.94]	.0245 ± .0005 [0.622]	.028 ± .001 [0.71]	.0075 Ref [0.191]	.035 [0.89]
05	.61 Ref [15.5]	.0250 ± .002 [0.635]	.035 ± .003 [0.90]	.003 Max [0.08]	.045 [1.14]

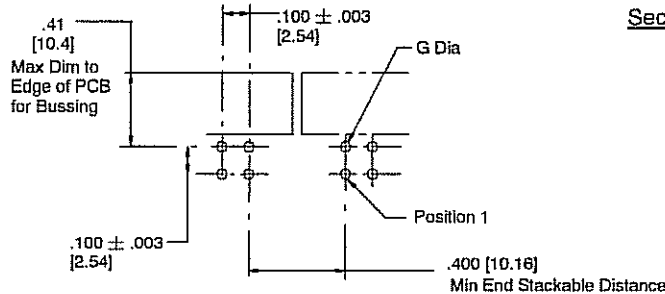
Pin Qty	Dimensions		Polarizing Notches
	A	B	
10	.788 [20.02]	.708 [17.98]	B C
14	.988 [25.10]	.908 [22.06]	B C D E
16	1.088 [27.64]	1.008 [25.60]	A B C D E
20	1.288 [32.72]	1.208 [30.68]	A B C D E
24	1.488 [37.80]	1.408 [35.76]	A B C D E
26	1.588 [40.34]	1.508 [38.30]	A B C D E
30	1.788 [45.42]	1.708 [43.38]	A B C D E
34	1.988 [50.50]	1.908 [48.46]	A B C D E
40	2.288 [58.12]	2.208 [56.08]	A B C D E
50	2.788 [70.82]	2.708 [68.78]	A B C D E
60	3.288 [83.52]	3.208 [81.48]	A B C D E
64	3.488 [88.60]	3.408 [86.56]	A B C D E



Right Angle



Section J-J



Recommended Mounting Hole Pattern

Notes:

- Notches "A" and "C" will accommodate 3M Polarizing Keys 3518.
- The recommended PCB hole size for the kinked tail positions on the .112" solder tail connector is .035" ± .002. Refer to TS-0972 for the position kinked.



Inch
[mm]

Tolerance Unless Noted			
	.0	.00	.000
Inch	± .1	± .01	± .005

[] Dimensions for Reference Only

Ordering Information

X25XX-50XXXX

Blank = Standard
N = High Temperature

Pin Quantity:
(See Table 1)

Tail

- 02 = Solder Tails for .062 [1.57] Thick Board.
- K2 = Kinked Solder Tails for .062 [1.57] Thick Board.
- 03 = Solder Tails for .094 to .125 [2.39 to 3.18] Thick Board.
- 05 = Wrap Tails for up to 3 Levels of Wire Wrap. (Normal temp only)

Mating Plating Thickness:

Solder Tail Versions

UG = 15 μ" [0.38 μm]

UB = 30 μ" [0.76 μm]

Wrap Tail Versions

EB = 30 μ" [0.76 μm]

(Normal temp Only)

TS-0770-11
Sheet 3 of 3

3M

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